WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a plurality of word lines;

a plurality of data line pairs;

a plurality of memory cells provided at the intersections between the plurality of word lines and the plurality of data line pairs;

the plurality of data line pairs including a first data line pair connected to a first data input/output line pair by a first select line and a second data line pair connected to the first data input/output line pair by a second select line;

a first sense amplifier connected to the first data line pair;

a second sense amplifier connected to the second data line pair;

a first switch comprising a first MISFET (metal insulator semiconductor field effect transistor) that is controlled by a first control line, and that is connected to a first node of the first sense amplifier to supply a first power source to the first sense amplifier; and

a second switch comprising a second MISFET that is controlled by the first control line, and that is connected to a second node of the second sense amplifier to supply the first power source to the second sense amplifier, wherein

the first node and the second node are electrically isolated from each other, and

at the time of writing data from the first data input/output line pair to the first data line pair, the first

select line is enabled earlier than the first control line.

2. The semiconductor device according to claim 1, further comprising:

a third sense amplifier connected to the first data line pair;

a fourth sense amplifier connected to the second data line pair;

a third switch comprising a third MISFET that is controlled by a second control line, and that is connected to a third node of the third sense amplifier to supply a second power source to the third sense amplifier; and

a fourth switch consisting of a fourth MISFET that is controlled by the second control line, and that is connected to a fourth node of the fourth sense amplifier to supply the second power source to the fourth sense amplifier, wherein

the plurality of word lines extend in a first direction, and the plurality of data line pairs extend in a second direction,

the first and second sense amplifiers have a first conductive MISFET pair respectively,

the third and fourth sense amplifiers have a second conductive MISFET pair respectively, and

the third node and the fourth node are electrically isolated from each other.

3. The semiconductor device according to claim 1, further

comprising:

a fifth MISFET that has a source and drain route between one data line of the first data line pair and one data input/output line of the first data input/output line pair, and a sixth MISFET that has a source and drain route between the other data line of the first data line pair and the other data input/output line of the first data input/output line pair, gates of the MISFETs being controlled by the first select line; and

a first output amplifier connected to the first data line pair, wherein

the first output amplifier comprises a seventh MISFET that has a source and drain route connected to a source and drain route of the fifth MISFET, an eighth MISFET that has a source and drain route connected to a source and drain route of the sixth MISFET, a ninth MISFET having the gate connected to one data line of the first data line pair and having the drain connected to a connection point between the drain of the sixth MISFET and the source of the eighth MISFET, and a tenth MISFET having the gate connected to the other data line of the first data line pair and having the drain connected to a connection point between the drain of the fifth MISFET and the source of the seventh MISFET, the MISFETS being controlled by a third control line respectively.

4. The semiconductor device according to claim 3, further comprising:

an eleventh MISFET that has a source and drain route between one data line of the second data line pair and one data input/output line of the first data input/output line pair, and a twelfth MISFET that has a source and drain route between the other data line of the second data line pair and the other data input/output line of the first data input/output line pair, gates of the MISFETs being controlled by the second select line;

a second output amplifier connected to the second data line pair,

a fifth switch controlled by a fourth control line and supplying a third power source to the first output amplifier connected to a fifth node; and

a sixth switch controlled by the fourth control line and supplying the third power source to the second output amplifier connected to a sixth node, wherein

the second output amplifier comprises a thirteenth MISFET that has a source and drain route connected to a source and drain route of the eleventh MISFET, a fourteenth MISFET that has a source and drain route connected to a source and drain route of the twelfth MISFET, a fifteenth MISFET having the gate connected to one data line of the second data line pair and having the drain connected to a connection point between the drain of the twelfth MISFET and the source of the fourteenth MISFET, and a sixteenth MISFET having the gate connected to the other data line of the second data line pair and having the drain connected to a connection point between the drain of the

eleventh MISFET and the source of the thirteenth MISFET, the MISFETS being controlled by the third control line respectively, and the fifth node and the sixth node being electrically isolated from each other.

5. The semiconductor device according to claim 1, wherein the plurality of data line pairs include a plurality of the first data line pairs that are controlled by the first select line, and

a plurality of the first sense amplifiers connected respectively to the first data line pairs share the first switch, and the memory cells connected to the first sense amplifiers have a MISFET and a capacitor respectively.

6. The semiconductor device according to claim 1, wherein the first data line pair connected to the first sense amplifier comprises complementary two lines that are connected with the memory cells, and the memory cells have a MISFET and a capacitor respectively.

7. The semiconductor device according to claim 2, wherein the first sense amplifier and the third sense amplifier, and the second sense amplifier and the fourth sense amplifier constitute positive feedback amplifiers respectively.

8. A semiconductor device comprising:

a plurality of word lines;

a plurality of data line pairs;

a plurality of memory cells that are provided at the intersections between the plurality of word lines and the plurality of data line pairs;

the plurality of data line pairs including a first data line pair connected to a first data input/output line pair by a first select line, and a second data line pair connected to the first data input/output line pair by a second select line;

a first sense amplifier connected to the first data line pair;

a second sense amplifier connected to the second data line pair;

a first switch comprising a first MISFET (metal insulator semiconductor field effect transistor) that is controlled by a first control line, and that is connected to a first node of the first sense amplifier to supply a first power source to the first sense amplifier; and

a second switch comprising a second MISFET that is controlled by the first control line, and that is connected to a second node of the second sense amplifier to supply the first power source to the second sense amplifier, wherein

when the word lines are enabled, data are read out to all the plurality of data line pairs, and

the first node and the second node are electrically isolated from each other.

9. The semiconductor device according to claim 8, further

comprising:

a third sense amplifier connected to the first data line pair;

a fourth sense amplifier connected to the second data line pair;

a third switch comprising a third MISFET that is controlled by a second control line, and that is connected to a third node of the third sense amplifier to supply a second power source to the third sense amplifier; and

a fourth switch consisting of a fourth MISFET that is controlled by the second control line, and that is connected to a fourth node of the fourth sense amplifier to supply the second power source to the fourth sense amplifier, wherein

the first and second sense amplifiers have a first conductive MISFET pair respectively,

the third and fourth sense amplifiers have a second conductive MISFET pair respectively,

the plurality of word lines extend in a first direction, and the plurality of data line pairs extend in a second direction, and

the third node and the fourth node are electrically isolated from each other.

10. The semiconductor device according to claim 8, further comprising:

a fifth MISFET that has a source and drain route between one data line of the first data line pair and one data

input/output line of the first data input/output line pair, and a sixth MISFET that has a source and drain route between the other data line of the first data line pair and the other data input/output line of the first data input/output line pair, gates of the MISFETs being controlled by the first select line; and

a first output amplifier connected to the first data line pair, wherein

the first output amplifier comprises a seventh MISFET that has a source and drain route connected to a source and drain route of the fifth MISFET, an eighth MISFET that has a source and drain route connected to a source and drain route of the sixth MISFET, a ninth MISFET having the gate connected to one data line of the first data line pair and having the drain connected to a connection point between the drain of the sixth MISFET and the source of the eighth MISFET, and a tenth MISFET having the gate connected to the other data line of the first data line pair and having the drain connected to a connection point between the drain of the fifth MISFET and the source of the seventh MISFET, the MISFETS being controlled by a third control line respectively.

11. The semiconductor device according to claim 10, further comprising:

an eleventh MISFET that has a source and drain route between one data line of the second data line pair and one data input/output line of the first data input/output line pair, and

a twelfth MISFET that has a source and drain route between the other data line of the second data line pair and the other data input/output line of the first data input/output line pair, gates of the MISFETs being controlled by the second select line;

a second output amplifier connected to the second data line pair,

a fifth switch controlled by a fourth control line and supplying a third power source to the first output amplifier connected to a fifth node; and

a sixth switch controlled by the fourth control line and supplying the third power source to the second output amplifier connected to a sixth node, wherein

the second output amplifier comprises a thirteenth MISFET that has a source and drain route connected to a source and drain route of the eleventh MISFET, a fourteenth MISFET that has a source and drain route connected to a source and drain route of the twelfth MISFET, a fifteenth MISFET having the gate connected to one data line of the second data line pair and having the drain connected to a connection point between the drain of the twelfth MISFET and the source of the fourteenth MISFET, and a sixteenth MISFET having the gate connected to the other data line of the second data line pair and having the drain connected to a connection point between the drain of the eleventh MISFET and the source of the thirteenth MISFET, the MISFETS being controlled by the third control line respectively, and the fifth node and the sixth node being electrically

isolated from each other.

12. A semiconductor device comprising:

a memory array, said memory including:

a first address latch for holding a first write address which is input according to a first write command;

a first write data latch for holding a first write data which is input according to the first write command; and

a first sub-memory array;

the first sub-memory array having;

a plurality of word lines extending in a first direction;

a plurality of data pair lines extending in a second direction; and

a plurality of memory cells;

the plurality of data line pairs including:

a first data line pair that is selected by a first select line corresponding to the first write address; and

a second data line pair that is selected by a second select line;

a first sense amplifier comprised of a first conductive MISFET pair provided in the first data line pair;

a second sense amplifier provided adjacent to the first sense amplifier and comprised of the first conductive MISFET pair provided in the second data line pair;

a first switch comprising the first conductive MISFET controlled by a first control line and connected to a first

node of the first sense amplifier to supply a first power source to the first sense amplifier; and

a second switch comprising the first conductive MISFET controlled by the first control line and connected to a second node of the second sense amplifier to supply the first power source to the second sense amplifier, wherein

the first node and the second node are electrically isolated from each other, and

a first word line corresponding to the first write address is selected according to a second write command that is input after the first write command, and the first write data is transferred to the first sense amplifier.

13. The semiconductor device according to claim 12, wherein

the plurality of memory cells have a MISFET and a capacity respectively,

a second write address that is input according to the second write command is transferred to the first address latch, and

a second write data that is input according to the second write command is transferred to the first write data latch.

14. The semiconductor device according to claim 12, further comprising:

a fifth MISFET that has a source and drain route between one data line of the first data line pair and one data input/output line of a first data input/output line pair, and a

sixth MISFET that has a source and drain route between the other data line of the first data line pair and the other data input/output line of the first data input/output line pair, gates of the MISFETs being controlled by the first select line; and

a first output amplifier connected to the first data line pair, wherein

the first output amplifier comprises a seventh MISFET that has a source and drain route connected to a source and drain route of the fifth MISFET, an eighth MISFET that has a source and drain connected to a source and drain route of the sixth MISFET, a ninth MISFET having the gate connected to one data line of the first data line pair and having the drain connected to a connection point between the drain of the sixth MISFET and the source of the eighth MISFET, and a tenth MISFET having the gate connected to the other data line of the first data line pair and having the drain connected to a connection point between the drain of the fifth MISFET and the source of the seventh MISFET, the MISFETS being controlled by a third control line respectively.

15. The semiconductor device according to claim 14, further comprising:

an eleventh MISFET that has a source and drain route between one data line of the second data line pair and one data input/output line of the first data input/output line pair, and a twelfth MISFET that has a source and drain route between the

other data line of the second data line pair and the other data input/output line of the first data input/output line pair, gates of the MISFETs being controlled by the second select line;

a second output amplifier connected to the second data line pair,

a fifth switch controlled by a fourth control line and supplying a third power source to the first output amplifier connected to a fifth node; and

a sixth switch controlled by the fourth control line and supplying the third power source to the second output amplifier connected to a sixth node, wherein

the second output amplifier comprises a thirteenth MISFET that has a source and drain route connected to a source and drain route of the eleventh MISFET, a fourteenth MISFET that has a source and drain route connected to a source and drain route of the twelfth MISFET, a fifteenth MISFET having the gate connected to one data line of the second data line pair and having the drain connected to a connection point between the drain of the twelfth MISFET and the source of the fourteenth MISFET, and a sixteenth MISFET having the gate connected to the other data line of the second data line pair and having the drain connected to a connection point between the drain of the eleventh MISFET and the source of the thirteenth MISFET, the MISFETS being controlled by the third control line respectively, and the fifth node and the sixth node being electrically isolated from each other.

16. The semiconductor device according to claim 12, wherein when the first word line is selected, memory cells are connected to the first and second data line pairs.

17. A semiconductor device comprising:

a memory array including:

a first address latch for holding a first write address which is input according to a first write command;

a first write data latch for holding a first write data which is input according to the first write command;

a second address latch for holding a second write address which is input according to a second write command that is input after the first write command;

a second write data latch for holding a second write data which is input according to the second write command; and

a first sub-memory array;

the first sub-memory array having:

a plurality of word lines extending in a first direction;

a plurality of data pair lines extending in a second direction; and

a plurality of memory cells;

the plurality of data line pairs including:

a first data line pair that is selected by a first select line corresponding to the first write address; and

a second data line pair that is selected by a second select line;

a first sense amplifier comprised of a first conductive MISFET pair provided in the first data line pair;

a second sense amplifier provided adjacent to the first sense amplifier and that comprised of the first conductive MISFET pair provided in the second data line pair;

a first switch comprising the first conductive MISFET is controlled by a first control line and connected to a first node of the first sense amplifier to supply a first power source to the first sense amplifier; and

a second switch comprising the first conductive MISFET controlled by the first control line and connected to a second node of the second sense amplifier to supply the first power source to the second sense amplifier, wherein

the first node and the second node are electrically isolated from each other, and

a first word line corresponding to the first write address is selected according to a second write command that is input after the first write command, and the first write data is transferred to the first sense amplifier.

18. The semiconductor device according to claim 17, wherein

in accordance with the third write command, the second write address is transferred to the first address latch, the second write data is transferred to the first write data latch, a third write address that is input according to the third

write command is transferred to the second address latch, and a third write data that is input according to the third write command is transferred to the second write data latch.

19. The semiconductor device according to claim 17, further comprising:

a fifth MISFET that has a source and drain route between one data line of the first data line pair and one data input/output line of a first data input/output line pair, and a sixth MISFET that has a source and drain route between the other data line of the first data line pair and the other data input/output line of the first data input/output line pair, gates of the MISFETs being controlled by the first select line; and

a first output amplifier connected to the first data line pair, wherein

the first output amplifier comprises a seventh MISFET that has a source and drain route connected to a source and drain route of the fifth MISFET, an eighth MISFET that has a source and drain route connected to a source and drain route of the sixth MISFET, a ninth MISFET having the gate connected to one data line of the first data line pair and having the drain connected to a connection point between the drain of the sixth MISFET and the source of the eighth MISFET, and a tenth MISFET having the gate connected to the other data line of the first data line pair and having the drain connected to a connection point between the drain of the fifth MISFET and the source of

the seventh MISFET, the MISFETS being controlled by a third control line respectively.

20. The semiconductor device according to claim 19, further comprising:

an eleventh MISFET that has a source and drain route between one data line of the second data line pair and one data input/output line of the first data input/output line pair, and a twelfth MISFET that has a source and drain route between the other data line of the second data line pair and the other data input/output line of the first data input/output line pair, gates of the MISFETs being controlled by the second select line;

a second output amplifier connected to the second data line pair,

a fifth switch controlled by a fourth control line and supplying a third power source to the first output amplifier connected to a fifth node; and

a sixth switch controlled by the fourth control line and supplying the third power source to the second output amplifier connected to a sixth node, wherein

the second output amplifier comprises a thirteenth MISFET that has a source and drain route connected to a source and drain route of the eleventh MISFET, a fourteenth MISFET that has a source and drain route connected to a source and drain route of the twelfth MISFET, a fifteenth MISFET having the gate connected to one data line of the second data line pair and

having the drain connected to a connection point between the drain of the twelfth MISFET and the source of the fourteenth MISFET, and a sixteenth MISFET having the gate connected to the other data line of the second data line pair and having the drain connected to a connection point between the drain of the eleventh MISFET and the source of the thirteenth MISFET, the MISFETS being controlled by the third control line respectively, and the fifth node and the sixth node being electrically isolated from each other.

21. The semiconductor device according to claim 17, wherein when the first word line is selected, memory cells are connected to the first and second data line pairs.

22. A semiconductor device comprising:

a circuit for holding an address;

a circuit for holding data;

a memory array including:

a plurality of word lines extending in a first direction;

a plurality of data line pairs extending in a second direction; and

a plurality of memory cells;

a first sense amplifier having a first conductive MISFET pair connected to a first data line pair among the plurality of data line pairs;

a second sense amplifier having the first conductive

MISFET pair provided in the second data line pair among the plurality of data line pairs;

a first switch having the first conductive MISFET controlled by a first control line and connected to a first node of the first sense amplifier to supply a first power source to the first sense amplifier; and

a second switch having the first conductive MISFET controlled by the first control line and connected to a second node of the second sense amplifier to supply the first power source to the second sense amplifier, wherein

the first and second sense amplifiers are provided adjacently,

a first address is input according to a first write command, a word line corresponding to a second address held in the address holding circuit is enabled by the first write command, a data held in the data holding circuit is transferred to the first data line pair corresponding to a second address, and

the first node and the second node are electrically isolated from each other.

23. The semiconductor device according to claim 22, further comprising:

a third sense amplifier having a second conductive MISFET pair connected to the first data line pair;

a fourth sense amplifier having the second conductive MISFET pair connected to the second data line pair;

a third switch controlled by a second control line and connected to a third node of the third sense amplifier to supply a second power source to the third sense amplifier; and

a fourth switch controlled by the second control line and connected to a fourth node of the fourth sense amplifier to supply the second power source to the fourth sense amplifier, wherein

a first data to be written into a memory cell corresponding to a first address is input according to the first write command, and

the third node and the fourth node are electrically isolated from each other.

24. A semiconductor device comprising:

a plurality of word lines;

a plurality of data line pairs;

a plurality of dynamic memory cells;

the plurality of data line pairs including a first data line pair connected to a first data input/output line pair by a first select line, and a second data line pair connected to the first data input/output line pair by a second select line;

a first sense amplifier that is connected to the first data line pair;

a second sense amplifier that is connected to the second data line pair;

a first switch comprising a first MISFET controlled by a first control line and connected to a first node of the first

sense amplifier to supply a first power source to the first sense amplifier; and

a second switch comprising a second MISFET controlled by the first control line and connected to a second node of the second sense amplifier to supply the first power source to the second sense amplifier, wherein

the first data line pair comprises complementary first and second data lines, the first and second data lines being connected with memory cells respectively,

the second data line pair comprises complementary third and fourth data lines, the third and fourth data lines being connected with memory cells respectively, and

the first node and the second node are electrically isolated from each other.

25. The semiconductor device according to claim 24, wherein

the memory cells connected to the first data line have a third MISFET and a capacitor connected to the third MISFET, the gate of the third MISFET being connected to a first word line among a plurality of word lines, and a source and drain route of the third MISFET being connected to the first data line, and

the memory cells connected to the second data line have a fourth MISFET and a capacitor connected to the fourth MISFET, the gate of the fourth MISFET being connected to the first word line, and a source and drain route of the fourth MISFET being connected to the second data line.

26. The semiconductor device according to claim 25, wherein

a plurality of first data line pairs are selected according to the first select line;

a plurality of second data line pairs are selected according to the second select line;

a plurality of first sense amplifiers connected to the plurality of first data line pairs share a first switch; and

a plurality of second sense amplifiers connected to the plurality of second data line pairs share a second switch.